| **Course Code: CS2006** | **Course Name: Operating Systems** | |
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| **Instructor Name: Dr. Ghufran Ahmed** | | **Issue Date: 26th April 2023** |
| **Assignment no. 04** | | **Due Date: May 5, 2023** |

**Instructions:**

* Assignment should be solved handwritten on paper and their scanned soft copies are to be submitted on GCR.
* Must write your NU id on the top of each page of the assignment.
* Rough work must be solved for the clarification of the answer.
* Prints of Soft copy documented assignment cost direct zero.
* **All questions have equal marks (5 Each) - Total Marks-30 Marks**

1. Consider a three-level paging scheme with a TLB. Assume no page fault occurs. It takes 30 ns to search the TLB and 100 ns to access the physical memory. If the TLB hit ratio is 70%, What will be its EAT??
2. Consider a demand-paging system with a paging disk that has average access and transfer time of 25 milliseconds. Addresses are translated through a page table in the main memory, with an access time of 1 microsecond per memory access. Thus, each memory reference through the page table takes two accesses. To improve this time, we have added an associative memory that reduces access time to one memory reference if the page-table entry is in the associative memory. Assume that 80 percent of the accesses are in the associative memory and that, of those remaining, 10 percent (or 2 percent of the total) cause page faults. What is the effective memory access time in milliseconds?
3. Consider the following page reference string:

1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.

How many page faults and page hits would occur for the following replacement algorithms, assuming three frames? Remember that all frames are initially empty, so your first unique pages will cost one fault each.

a) LRU replacement

b) Optimal replacement

c) Second Chance

1. Consider a computer system with a 32-bit logical address and 4-KB page size. The system supports up to 512 MB of physical memory. How many entries are there in each of the following?
2. Calculate the size of memory if its address consists of 22 bits and the memory is 2-byte addressable.
3. Given the following statement for banker algorithm:

6 Processes P0 through P5

4 Resource Types A (15 instances) B(6 instances) C(9 instances) D(10 instances)

Snapshot at Time T0:8

1. Calculate the need matrix
2. Show the safe sequence of processes. In addition to the sequence show the Available (Work Array) changes as each process terminates